AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-29. (cancelled)

30. (new) A semiconductor package comprising:

a planar mounting element;

a semiconductor chip having a bottom surface on which a first electrode is formed, and a top surface on which a second electrode and a third electrode are formed, said semiconductor chip being mounted on said planar mounting element such that the first electrode of said bottom surface is in electrical contact with said planar mounting element;

a first lead element having a first inner portion and a first outer portion, said first inner portion extending from said planar mounting element and electrically connected to said first electrode via said planar mounting element;

a second lead element having a second inner portion and a second outer portion, said second inner portion being bonded and electrically connected to said second electrode;

a third lead element having a third inner portion and a third outer portion, said third inner portion being positioned above and spaced apart from said top surface of said semiconductor chip;

a bonding wire element electrically connecting between said third inner portion and said third electrode; and

an enveloper encapsulating said planar mounting element, said semiconductor chip, said bonding wire element, and said first, second and third inner portions of said first, second and third lead elements.

31. (new) The semiconductor package as set forth in claim 30, wherein said first, second and third outer portions of said first, second and third lead elements are projected outward from said enveloper.

32. (new) The semiconductor package as set forth in claim 30, wherein said first, second and third outer portions of said first, second and third lead elements are substantially arranged so as to be coplanar with each other.

33. (new) The semiconductor package as set forth in claim 30, wherein said second inner portion of said second lead element is bonded to said second electrode with electrically-conductive paste (BM).

34. (new) The semiconductor package as set forth in claim 30, wherein said semiconductor chip comprises a MOSFET chip in which said respective first, second and third electrodes are formed as drain, source and gate electrodes.

35. (new) The semiconductor package as set forth in claim 30, wherein said second electrode has a larger area than that of said third electrode.

36. (new) The semiconductor package as set forth in claim 30, wherein said first outer portion of said first lead element is projected from a first side face of said enveloper, said second and third outer portions of said second and third lead elements are projected from a second side face opposed to said first side face of said enveloper.

37. (new) The semiconductor package as set forth in claim 30, wherein one surface of said planar mounting element, which is opposed to another surface thereof on which said semiconductor chip is mounted, is exposed out of said enveloper.

38. (new) The semiconductor package as set forth in claim 37, wherein the exposed surface of said planar mounting element is substantially coplanar with respect to said second and third outer portions of said second and third lead elements.

39. (new) A semiconductor package comprising:

a plate-like mount;

a semiconductor chip having a first electrode formed on a bottom surface thereof, and a second electrode and a third electrode formed on a top surface thereof, said semiconductor chip being mounted on said plate-like mount such that said first electrode is in electrical contact with said planar mounting element;

a first lead element integrally extending from said plate-like mount and electrically connected to said first electrode via said plate-like mount;

a second lead element being bonded and electrically connected to said second electrode at an inner end thereof;

a third lead element having an inner end which is positioned above and spaced apart from said third electrode;

a bonding wire element electrically connecting between said third inner portion and said third electrode; and

a molded resin enveloper sealing and encapsulating said plate-like mount, said semiconductor chip, and said bonding wire element so that respective outer end portions of said first, second and third lead elements extending out of said molded resin enveloper.

40. (new) The semiconductor package as set forth in claim 39, wherein said outer portions of said first, second and third lead elements are substantially arranged so as to be coplanar with each other.

41. (new) The semiconductor package as set forth in claim 39, wherein said inner end of said second lead element is bonded to said second electrode with electrically-conductive paste (BM).

42. (new) The semiconductor package as set forth in claim 39, wherein said semiconductor chip comprises a MOSFET chip on which said respective first, second and third electrodes are formed as drain, source and gate electrodes.

43. (new) The semiconductor package as set forth in claim 39, wherein said second electrode has a larger area than that of said third electrode.

44. (new) The semiconductor package as set forth in claim 39, wherein said outer portion of said first lead element is projected from a first side face of said molded resin enveloper, said outer portions of said second and third lead elements are projected from a second side face opposed to said first side face of said molded resin enveloper.

45. (new) The semiconductor package as set forth in claim 39, wherein one surface of said plate-like mount, which is opposed to another surface thereof on which said semiconductor chip is mounted, is exposed out of said molded resin enveloper.

46. (new) The semiconductor package as set forth in claim 45, wherein the exposed surface of said plate-like mount is substantially coplanar with respect to said outer portions of said second and third lead elements.